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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/810,672	03/29/2004	Masamichi Fujito	XA-10065	1157

181 7590 05/09/2006

MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
SUITE 500
MCLEAN, VA 22102-3833

EXAMINER	
PHAN, TRONG Q	
ART UNIT	**PAPER NUMBER**
2827	

DATE MAILED: 05/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/810,672	FUJITO ET AL.	
	Examiner	Art Unit	
	TRONG PHAN	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2006*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☒ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *21-25* is/are withdrawn from consideration.

5)☒ Claim(s) *1-20* is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: **41, n+, n-, p+, p- and p-Sub in Fig. 3; CBL, TRG, SPC(L), SPC(R), SEN(L), SEN(R), SA(L) and SA(R) in Fig. 5; SPC(L), SPC(R), SEN(L) and SEN(R) in Fig. 6); SPC(L) <READ>, SPC(R) <REFERENCE>, CCS <COMPARISON CURRENT SELECTION>, CCS(T), CBL(B) <REFERENCE>, CBL(T) <READ>, SEN(L) <READ>, SEN(R) <REFERENCE>, GBLr(R) <REFERENCE> and GBLr(L) <READ> in Fig. 7; SPC(L), SPC(R), SEN(L), SEN(R), SA(L) and SA(R) in Fig. 8; WL (WRITE), GBLw (WRITE), WL (READ) and GBLr (READ) in Fig. 12; SA(L), SA(R), WLa, WLb, WLc, WLd, SPCa, SPCb, SPCc, SPCd, SENa, SENb, SENc and SENd in Fig. 16; WLa, WLb, WLc, WLd, SPCa, SPCb, SPCc, SPCd, SENa, SENb, SENc and SENd in Figs. 17-18; GBLrDRVc, GBLrDRVd, SA(L), SA(R), WLa, WLb, WLc, WLd, SPCa, SPCb, SPCc, SPCd, SENa, SENb, SENc and SENd in Fig. 19; RDECab in Fig. 20; SPC (L), CCS (T), CBL (T), CBL (B), CCB, CCS (B), SEN (L) and SA(L) in Fig. 22; SA (L), GBLv [VERIFY GBL] and GBLr [READ GBL] in Figs. 25 and 27; CMP (VERIFY COMPARATOR) in Fig. 28; CBL (T), CBL (B), CCB, CCS (B), SPC (L), CCS (T), CCS (B), [READ GBL] and [VERIFY GBL] in Fig. 29**. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any

amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claims 13-14, 16-17, and 19-20 are objected to because of the following informalities:

Claim 13, no antecedent basis for "the change " (lines 6 and 8) and "the number of cycles"(lines 6-7).

Claim 14, no antecedent basis for "the next address" (line 5) and "the respective" (line 7).

Claim 16, no antecedent basis for "the remaining" (line 5).

Claim 17, no antecedent basis for "said first bit line" (line 9), "the number" (line 10), "said second bit lines" (line 10) and "the parallel write bit number" (line 11).

Claim 19, no antecedent basis for "dis-coupling" (line 6). This operation should be further defined.

Claim 20, no antecedent basis for "the first bit lines of the plurality of memory arrays" (lines 7-8) and "said first bit line" (line 9).

Appropriate correction is required.

Allowable Subject Matter

3. Claims 1-20 are allowed.

4. The following is an examiner's statement of reasons for allowance:

The nonvolatile memory device enabling electric erase and write over a semiconductor substrate comprising a plurality of blocks each having a plurality of first bit lines, a plurality of second bit lines and a plurality of third bit lines and a plurality of first amplifiers wherein: each of first bit lines is coupled with an input terminal of a corresponding one of the first amplifiers, each of second bit lines is coupled with an output terminal of a corresponding one of the first amplifiers and each of the third bit lines is selectively coupled with a corresponding of the first bit lines and is used for transferring data to be written into a memory cell as recited in claims 1-16 has not been found in the prior art.

The nonvolatile memory device comprising a nonvolatile memory enabling electric erase and write, a central processing unit capable of accessing the nonvolatile memory on a semiconductor substrate, wherein: the nonvolatile memory comprising a hierarchal bit line structure including first bit lines, a second bit line, a sense amplifier arranged the first bit lines and the second bit line and a number of the second bit lines is smaller the parallel write bit number to the memory array as recited in claims 17-19 has not been found in the prior art.

The semiconductor integrated circuit comprising a nonvolatile memory enabling electric erase and write on a semiconductor substrate wherein the nonvolatile memory comprising a hierarchal bit line structure including first bit lines specific to each of a

plurality of memory arrays, a second bit lines shared between the first bit lines and a sense amp selectively amplifying data read from the first bit lines to output the amplified data to the second bit line as recited in claim 20 has not been found in the prior art.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

5. This application is in condition for allowance except for the following formal matters: objections to the drawings of the present invention and claims 13-14, 16-17, and 19-20.

Prosecution on the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

A shortened statutory period for reply to this action is set to expire **TWO MONTHS** from the mailing date of this letter.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to TRONG PHAN whose telephone number is (571) 272-1794. The examiner can normally be reached on M-F (8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, AMIR ZARABIAN can be reached on (571)272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TRONG PHAN
PRIMARY EXAMINER

Approved
TP
5/2/06

FIG. 9

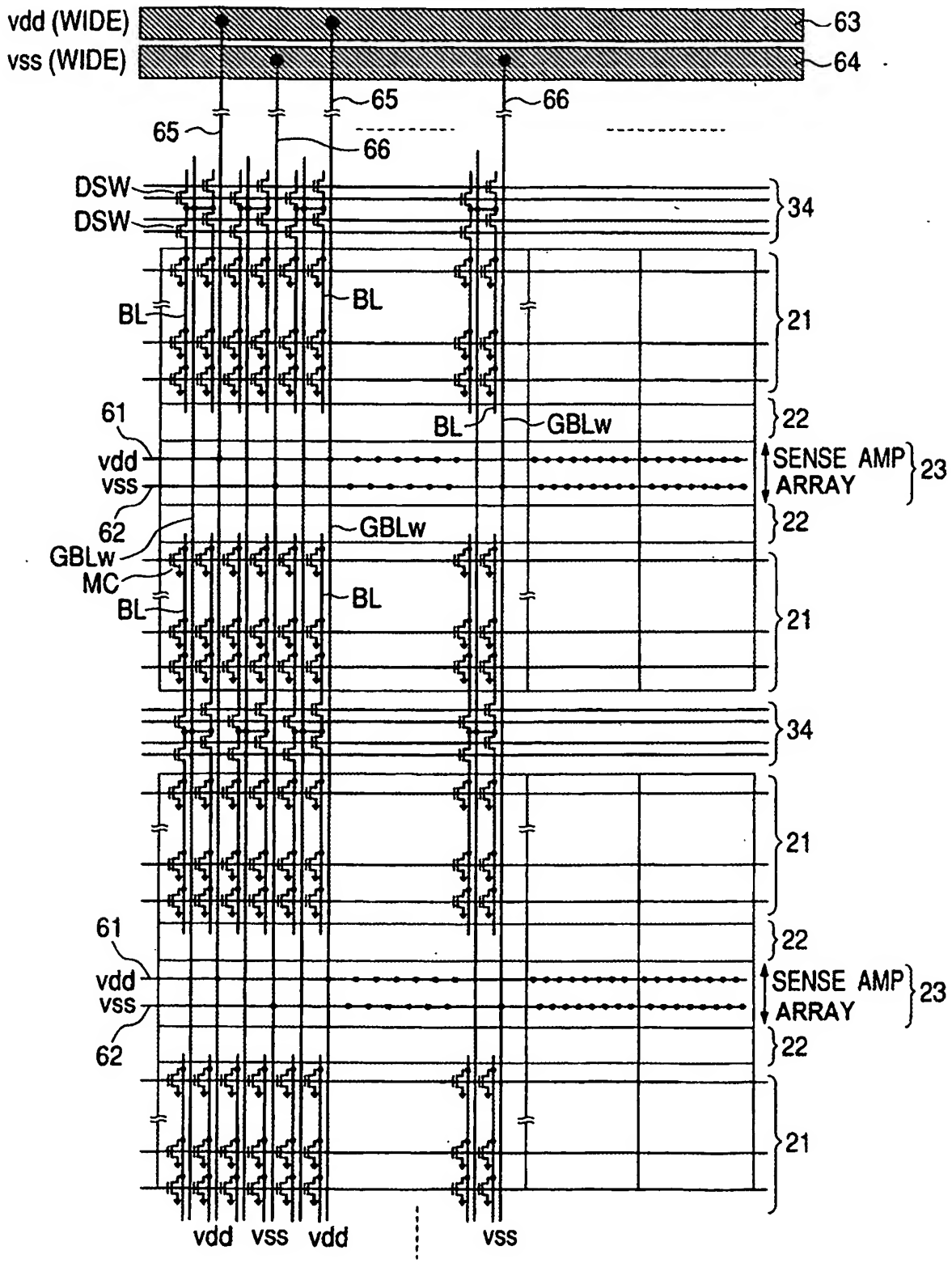


FIG. 10

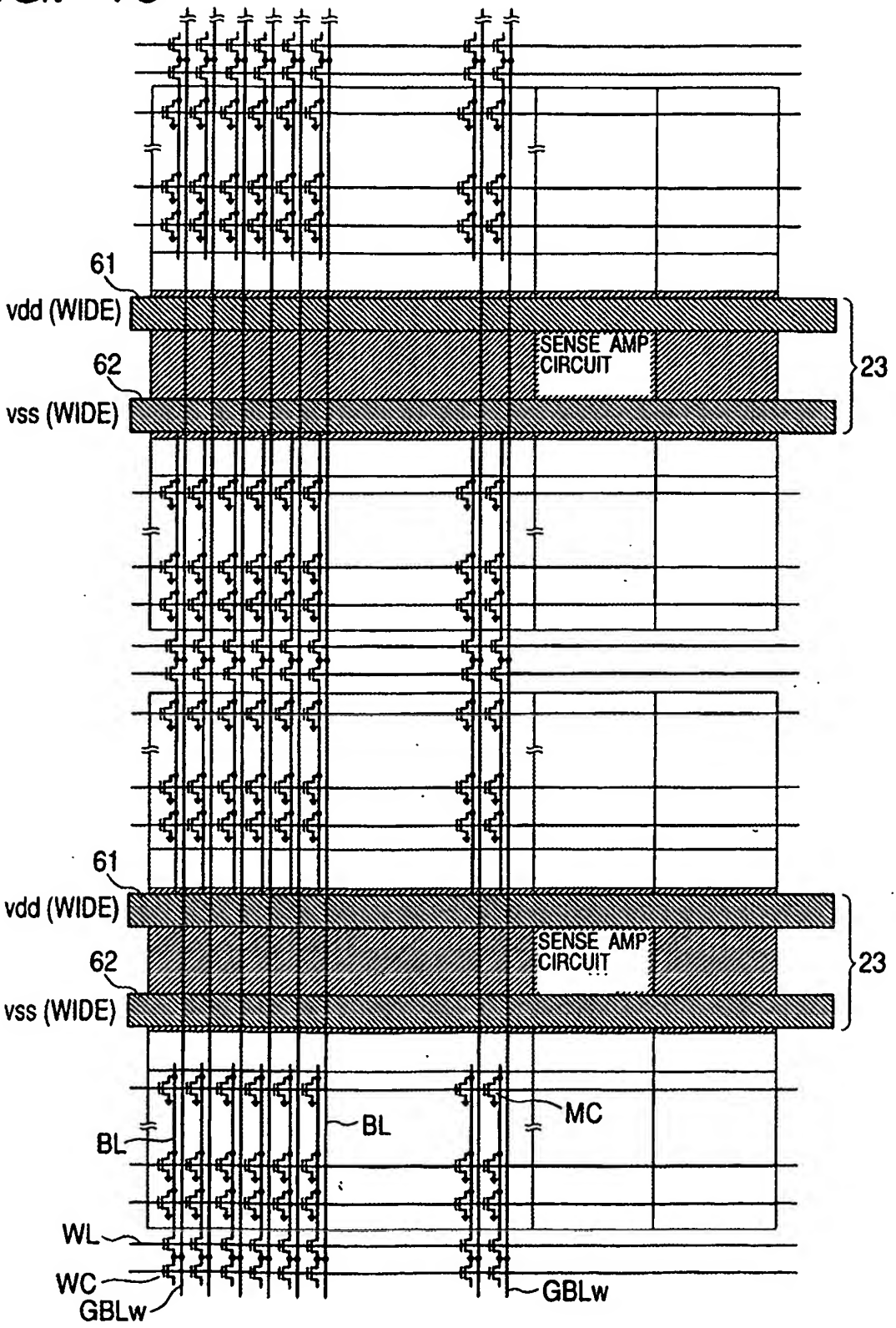

61
vdd (WIDE)
62
vss (WIDE)
SENSE AMP CIRCUIT
23
61
vdd (WIDE)
62
vss (WIDE)
SENSE AMP CIRCUIT
23
BL
BL
MC
WL
WC
GBLw
GBLw

FIG. 14

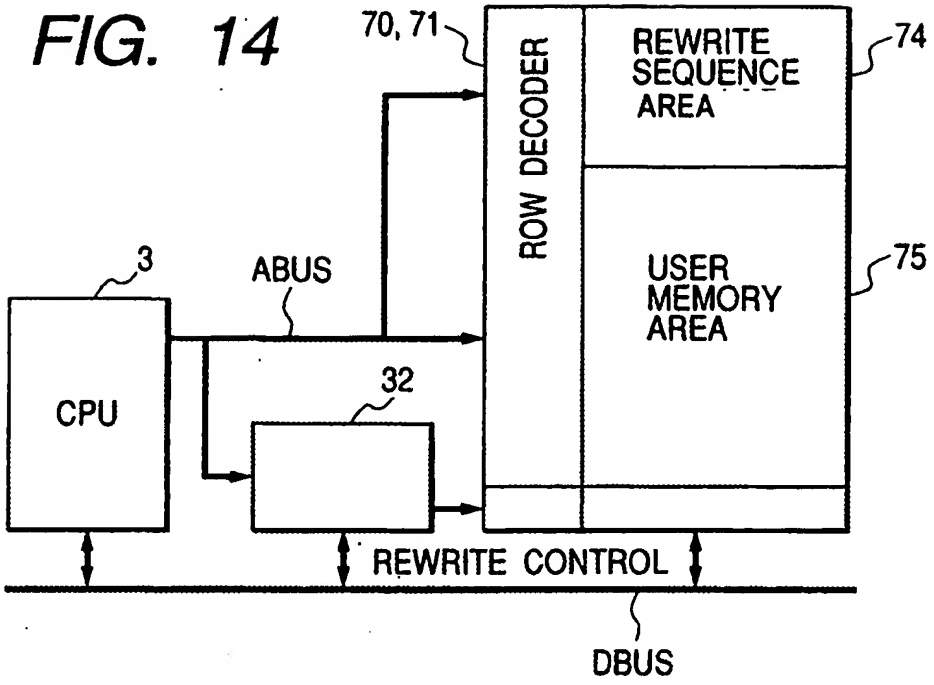

70, 71
ROW DECODER
REWRITE SEQUENCE AREA
74
USER MEMORY AREA
75
3
ABUS
CPU
32
REWRITE CONTROL
DBUS

FIG. 15

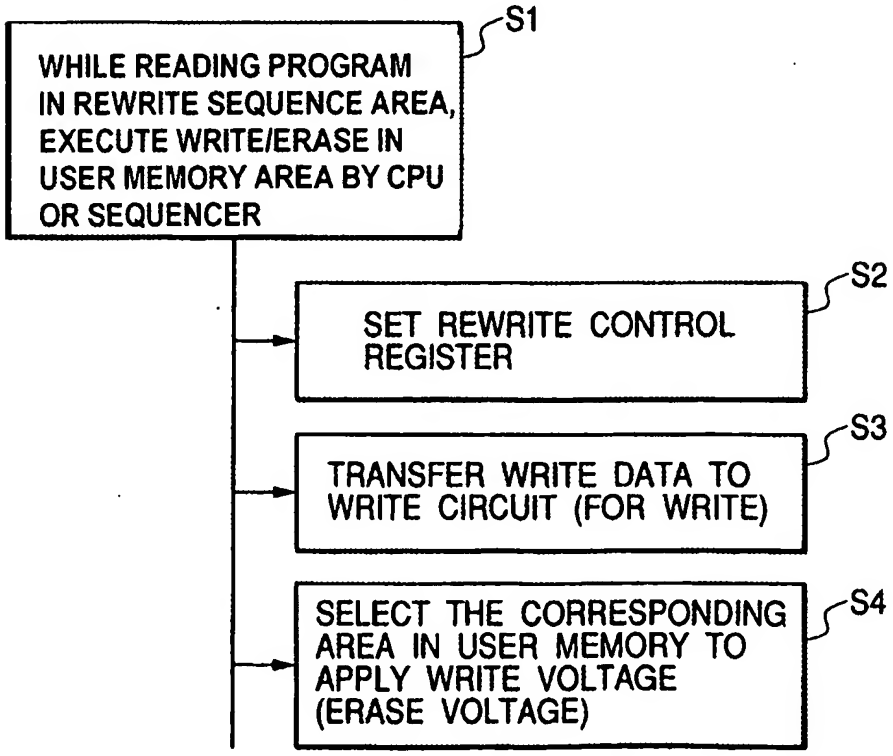

S1
WHILE READING PROGRAM IN REWRITE SEQUENCE AREA, EXECUTE WRITE/ERASE IN USER MEMORY AREA BY CPU OR SEQUENCER
S2
SET REWRITE CONTROL REGISTER
S3
TRANSFER WRITE DATA TO WRITE CIRCUIT (FOR WRITE)
S4
SELECT THE CORRESPONDING AREA IN USER MEMORY TO APPLY WRITE VOLTAGE (ERASE VOLTAGE)

FIG. 17

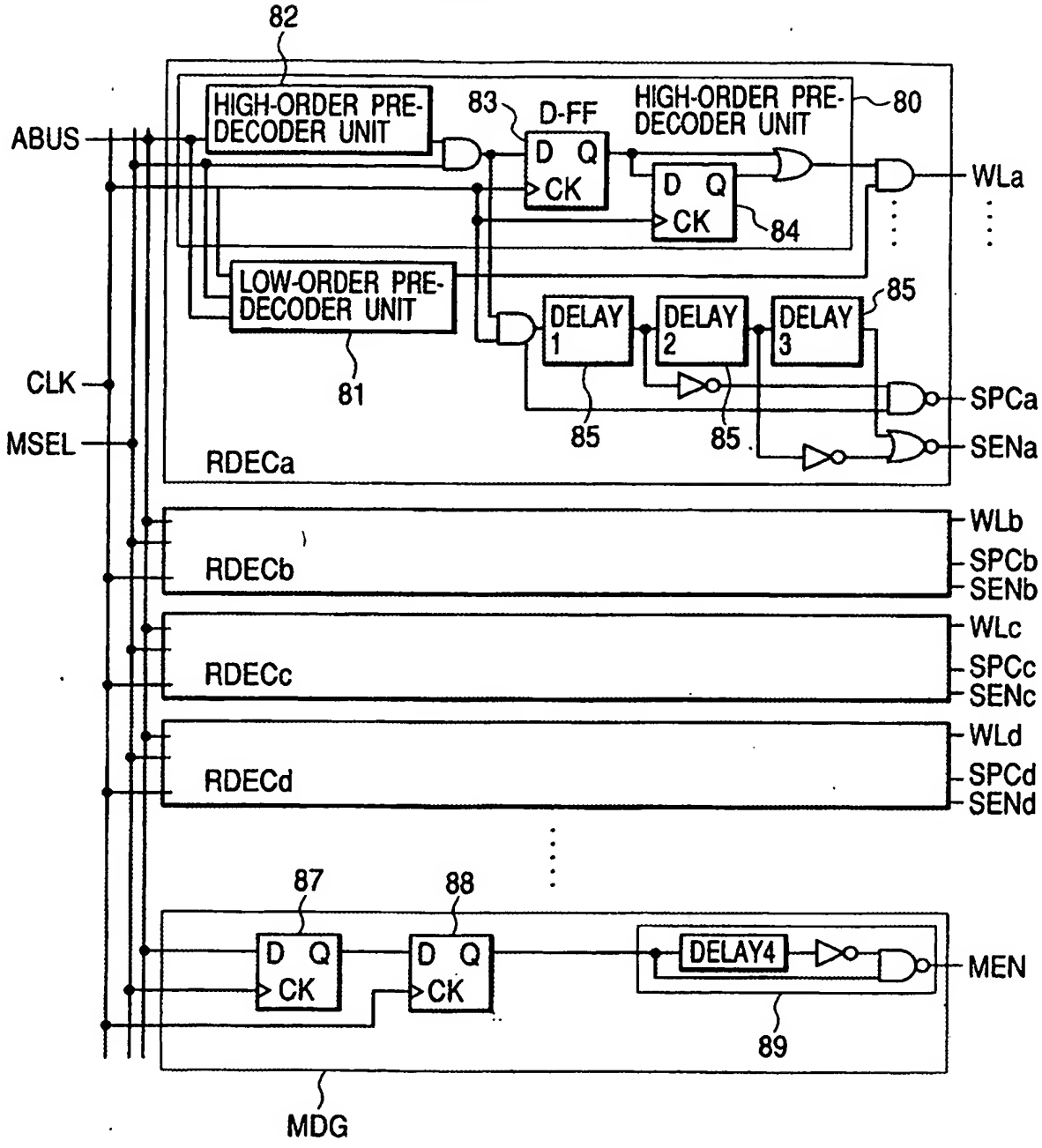

82
HIGH-ORDER PRE-DECODER UNIT
83
D-FF
HIGH-ORDER PRE-DECODER UNIT
80
ABUS
D Q
CK
D Q
CK
84
WLa
LOW-ORDER PRE-DECODER UNIT
DELAY 1
DELAY 2
DELAY 3
85
CLK
81
SPCa
MSEL
85
85
SENa
RDECa
WLb
RDECb
SPCb
SENb
WLc
RDECc
SPCc
SENc
WLd
RDECd
SPCd
SENd
87
88
D Q
CK
D Q
CK
DELAY4
MEN
89
MDG

FIG. 18

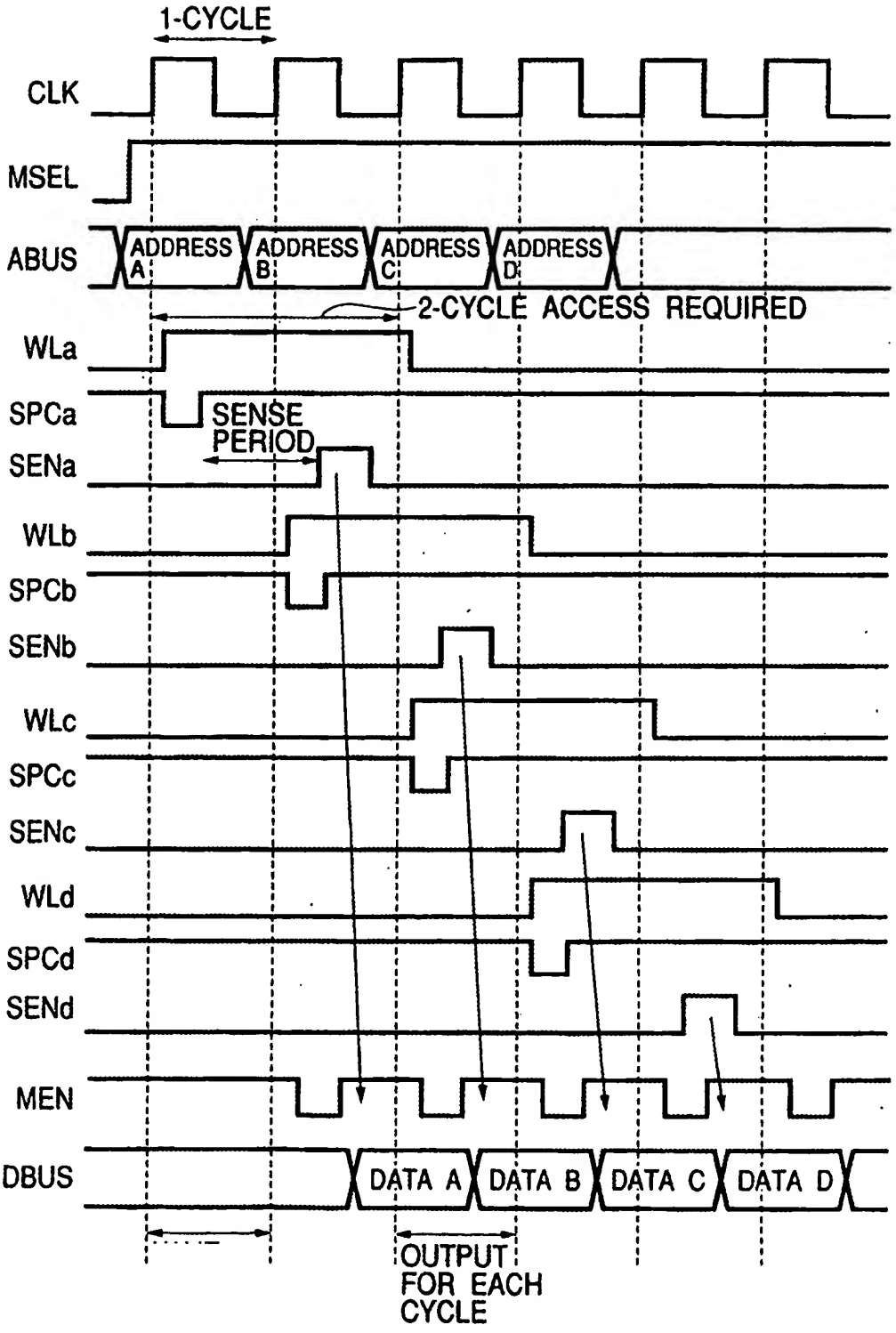

1-CYCLE
CLK
MSEL
ABUS
ADDRESS A
ADDRESS B
ADDRESS C
ADDRESS D
2-CYCLE ACCESS REQUIRED
WLa
SPCa
SENSE PERIOD
SENa
WLb
SPCb
SENb
WLc
SPCc
SENc
WLd
SPCd
SENd
MEN
DBUS
DATA A
DATA B
DATA C
DATA D
OUTPUT FOR EACH CYCLE

FIG. 21

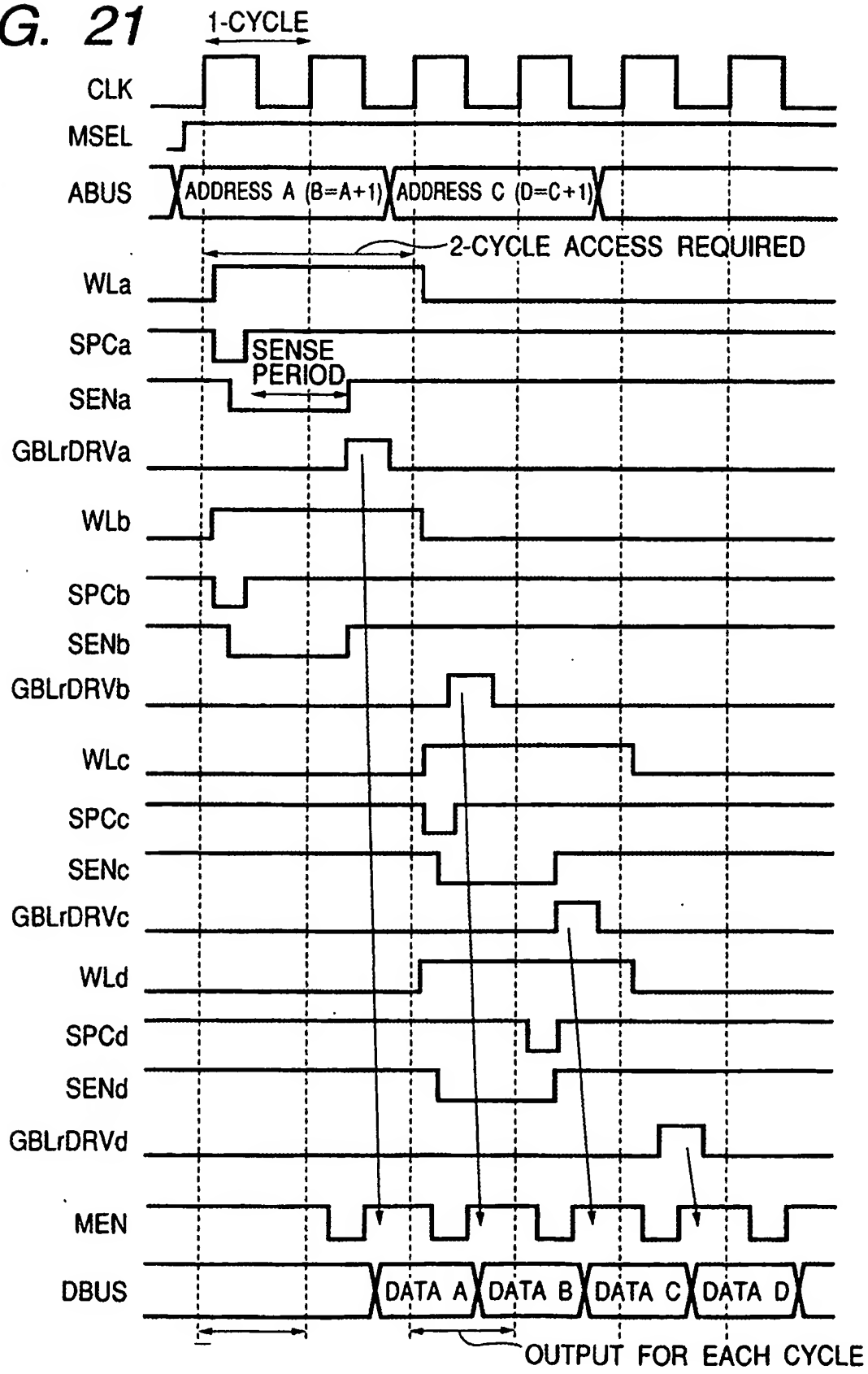
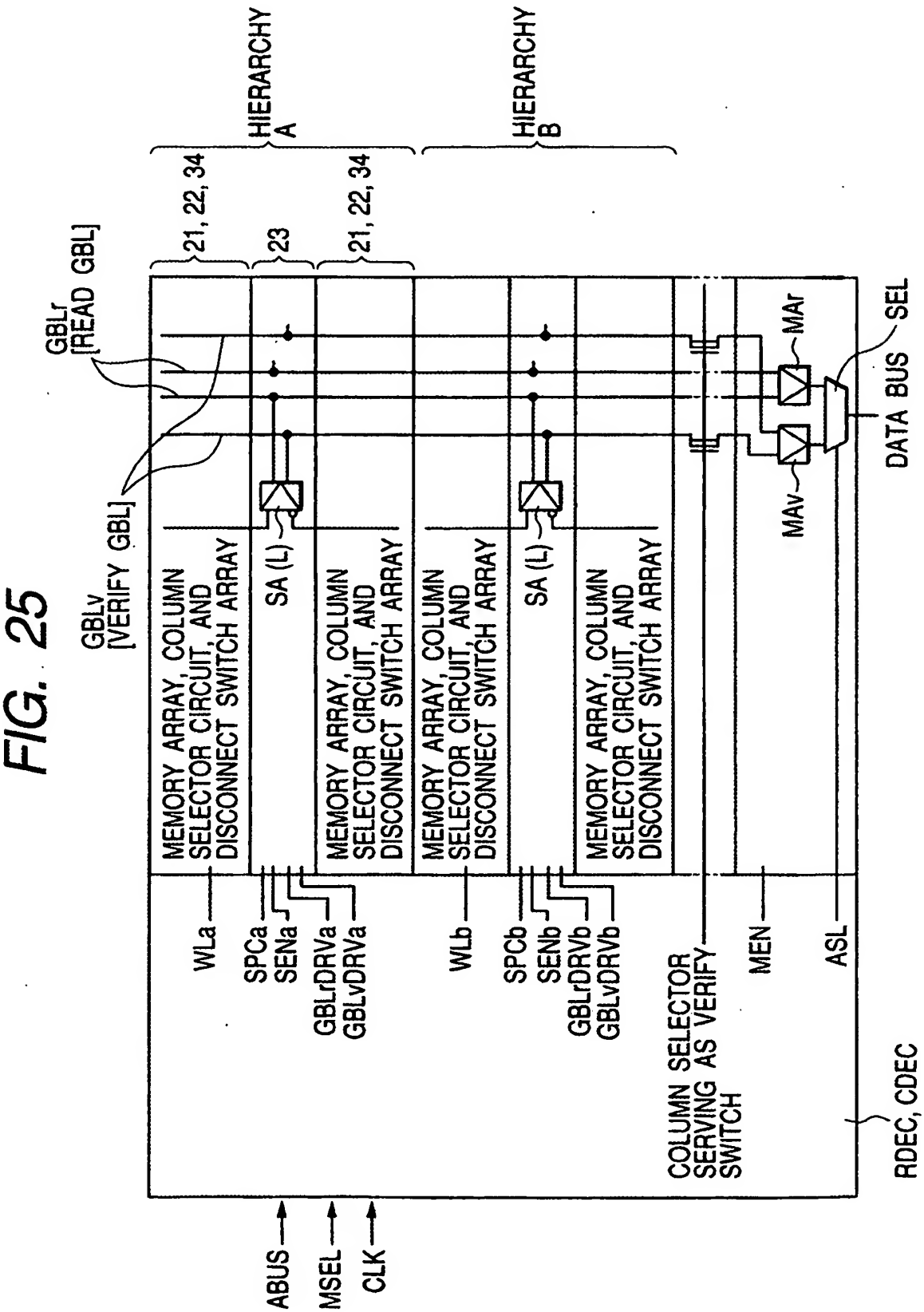

1-CYCLE
CLK
MSEL
ABUS
ADDRESS A (B=A+1)
ADDRESS C (D=C+1)
2-CYCLE ACCESS REQUIRED
WLa
SPCa
SENSE PERIOD
SENa
GBLrDRVa
WLb
SPCb
SENb
GBLrDRVb
WLc
SPCc
SENc
GBLrDRVc
WLd
SPCd
SENd
GBLrDRVd
MEN
DBUS
DATA A
DATA B
DATA C
DATA D
OUTPUT FOR EACH CYCLE

FIG. 25


HIERARCHY A
HIERARCHY B
21, 22, 34
23
21, 22, 34
GBLr [READ GBL]
GBLv [VERIFY GBL]
MEMORY ARRAY, COLUMN SELECTOR CIRCUIT, AND DISCONNECT SWITCH ARRAY
SA (L)
MAr
MAv
SEL
DATA BUS
WLa
SPCa
SENa
GBLrDRVa
GBLvDRVa
WLb
SPCb
SENb
GBLrDRVb
GBLvDRVb
COLUMN SELECTOR SERVING AS VERIFY SWITCH
MEN
ASL
RDEC, CDEC
ABUS
MSEL
CLK